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Design of Look up Table for Emerging Non Volatile Memories in FRAM

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Abstract: Non Volatile Memories (NVMs) can be used to implement the RAM cell in the lookup table. Here we proposed the four blocks non volatile single stage sense amplifier with voltage clamp is employed to reduce the power and area. One Transistor One Capacitor (1T1C) cell provides sufficient sense margin as a configuration bit and a Capacitor. Matched reference path is proposed to reduce the parasitic mismatch for reliable sensing. Tree multiplexer can be used non volatile memories in lookup table.

Index terms: non volatile memory, ferromagnetic memory, matched reference path.

1. INTRODUCTION

Density and increasing the integration cost of FPGAs. Emerging NVMs, such as MRAM, PRAM, and RRAM, have been verified with better scalability and logic compatibility. Based on the logic-in-memory concept, lookup table, which is the core building block in FPGAs, has been proposed with non volatility.[6,7] First, various nonvolatile SRAM (nvSRAM) structures with MRAM andRRAMwere proposed to directly replace SRAM in the traditional lookup table to acquire non volatility .However, the size of nvSRAM cell is remarkably larger than that of SRAM, and the write disturbance is also difficult to avoid for half-select RRAM cells[4,5]. Suzuki et al. also proposed a six-input nvLUT with serial/parallel magnetic junctions to acquire enough sensing margin. Ren proposed a third type of MRAM-based nvLUT named hybrid-LUT2. However, the ROFF/RON of MRAM is smaller compared with PRAM or RRAM, resulting in less sense margin or larger area due to serial/parallel magnetic junctions. Moreover, the first three MRAM nvLUTs have a mismatch in parasitic RC between the selected path in the multiplexer and the reference path, which may cause nvLUT to fail. For hybrid The basic low power design techniques, such as clock gating for reducing dynamic power, or multiple voltage thresholds to decrease leakage current, are well-established and supported by existing tools. In the past, the major concerns of the VLSI designer were area performance, cost and reliability. Power consideration was mostly of only secondary importance in recent years, however this has begun to change and increasingly power is being given comparable weight to area and speed consideration. several factors have contributed to this trend perhaps the primary driving factor has been the remarkable success and growth of the class of personal computing devices(audio and video based multimedia products)and wireless communication systems(personal digital assistants and personal communications)which demand high speed computation and complex functionality with low power consumption. In this application average power consumption is a critical design concern.SRAM-based field-programmable gate arrays (FPGAs) have been widely used during the last decades. However, the volatility of SRAM has limited FPGAs in applications where high security and instant power-on are required[3,9]. The problem can be solved by introducing nonvolatile memory (NVM) as the configuration bit. However, the traditional NVM devices, such as antifuse, E^2PROM, and flash, require high-voltage process and have poor logic compatibility. thus limiting the logic -LUT2, the configuration of MRAM cells shares the same decoding circuit with logic operation, whose inputs may be wired to other logic blocks and cannot be used as the address inputs during configuration. For RRAM, Sakamoto et al[11,15] proposed an nvLUT based on nanobridge. However, the programming path of nanobridge shares the same multiplexer with the logic path for selection, making the size of transistors in the multiplexer considerably large to satisfy the reset voltage for RON. Chen et al. Proposed another RRAM-based nvLUT using crossbar array. However, the sneaking paths inherent in crossbar array bring considerable leakage and poor sensing margin of only 10 mV.[7,8] To sum up, none of the previous work has achieved high reliability against memory and logic variations, low power, high-area efficiency, and low leakage at the same time. This brief introduces a low-power variation-tolerant nv LUT circuit to overcome the issues in the previous work. Because of its large ROFF/RON, 1T1R RRAM cell is used as a configuration bit and a reference resistor to provide sufficient sense margin against memory and logic variations. Thus, the area cost is decreased because no parallel or serial memory cell combinations are needed to guarantee the sense margin. To reduce the power and area, single-stage sense amplifier with voltage clamp (SSAVC) is employed without compromising the reliability. Moreover, matched reference path (MRP) is devised to minimize the parasitic RC

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mismatch between the selected path in the multiplexer and the reference path for reliable sensing against logic variations.

2. EXISTING SYSTEM

EXISTING LOW-POWER VARIATION-TOLERANT nvLUT

To illustrate the proposed design, a two-input nvLUT is presented.The input count can also be easily extended to six, which is prevailing in current main-stream FPGA products . The overall architecture of nvLUT consists of an SSAVC, a tree multiplexer (TMUX), an MRP, a RRAM slice, and a footer transistor. The RRAM slice constitutes of four 1T1R RRAM cells at the left for configuration and a dummy RRAM cell at the right-most as a reference resistor. The truth table is stored in the RRAM slice in the form of resistance state, ROFF or RON, which is different from the logic voltage in SRAM. For example, in order to program the nvLUT as a NOR gate, R0 should be programmed as RON denoting , while R1, R2, and R3 should be programmed as ROFF denoting 0. The inputs IN0 and IN1 select the corresponding RRAM cell through TMUX. To perform the operations of LUT, the sense amplifier is employed to convert the resistance state of RRAM cell into logic voltage. The function of footer transistor MF is to allow current to flow during sensing and it is closed during precharge to restrain leakage.

NON VOLATILE LOOKUP TABLE DESIGN IN RRAM CELL:

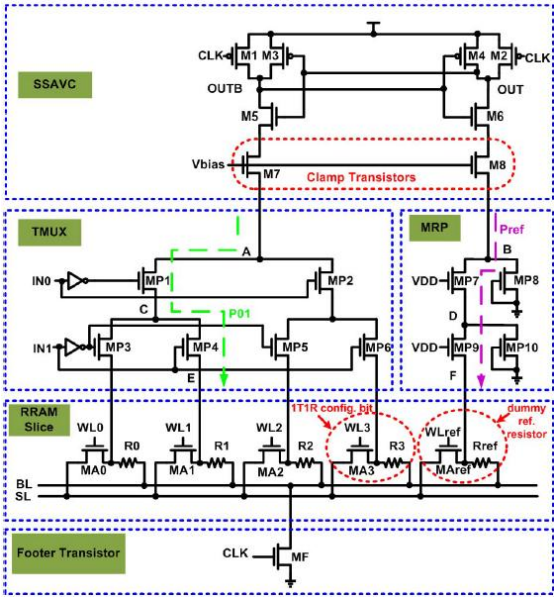

Fig 1 NON VOLATILE MEMORY IN RRAM

3. PROPOSED SYSTEM

3.1 PROPOSED IN NON VOLATILE MEMORY IN FRAM CELL:

SINGLE-STAGE SENSE AMPLIFIER WITH VOLTAGE CLAMP (SSAVC)

SSAVC converts the resistance state of FRAM into a rail-to-rail logic voltage. transistors M3–M6 constitute of a latch amplifier. Transistors M1 and M2 are used to precharge the output nodes OUT and OUTB to VDD when CLK is low and transistor MF is used to initiate the conversion when CLK is high. Compared with the previous two-stage sense amplifier , the single-stage realization occupies less die area. The internal voltages in TMUX and MRP are clamped to lower voltages by the clamp transistors to save power. In previous work, the inner nodes of the selected path in multiplexer and reference path are both precharged to VDD or (VDD-Vth) when CLK is low . Then, the charges are discharged to a capacitor or ground when CLK is high, resulting in considerable power waste. To alleviate this issue, transistors M7 and M8 are inserted between the sense amplifier and the TMUX/MRP. By applying a proper clamp voltage Vbias, which is lower than VDD, on the gates of M7 and M8, the inner nodes of the selected path in TMUX and MRP can only be precharged to (Vbias-Vth). In an FPGA chip, Vbias for different nvLUTs can be generated by a single voltage regulator with negligible overhead and it can also be tuned for different PVT conditions. Because of the quadratic relationship between energy and voltage, considerable average power saving can be achieved by the

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reduction of precharge voltage. Although the voltage clamp may incur reduced currents into the sense amplifier, large OFF/ON of FRAM still helps to preserve the sense margin without impairing the reliability.

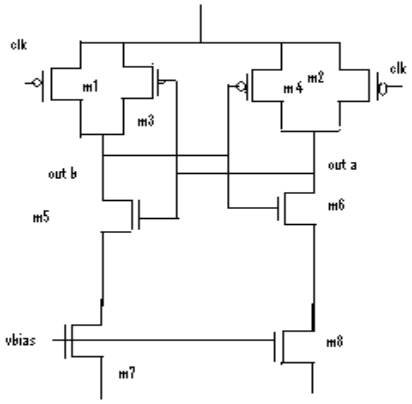

FIG 2 :SSAVC

3.2 MATCHED REFERENCE PATH (MRP)

Although trimming Cref by SAWM can help to disabuse the parasitic resistance mismatch between the selected path in TMUX and the reference path, their parasitic capacitance mismatch cannot be easily estimated and compensated. The MRP is devised to minimize the parasitic RC mismatch between the above-mentioned two paths. To illustrate this point, IN0 and IN1 are assumed to take the logic values of 0 and 1, respectively. The path marked by the green dash line in TMUX, P01, is selected to be compared with the reference path, Pref . For reliable sensing, the parasitic RCs of P01 and Pref should be equivalent. Therefore, the transistors MP8 and MP10 with their gate grounded are, respectively, added at the nodes B and D in MRP to imitate the parasitic effects of OFF-state transistors MP2 and MP3 at the nodes A and C in TMUX. Moreover, the transistors in MRP take the same size with the pass transistors in TMUX. Compares the parasitic RC of MRP with P01. It is assumed that the ON-state resistance of the pass transistor is Rp, the drain or source parasitic capacitance of the pass transistor is Cp, and the drain parasitic capacitance of the access transistor in the 1T1C FRAM cell is Ca .According to the Elmore delay formula, the RC time constant from node A/B/B' to node E/F/F' can be calculated as follows:

$t_{AE} = 5\ Rp * Cp + 2\ Rp * Ca$

$t_{BF} = 5\ Rp * Cp + 2\ Rp * Ca$

$t_{B'F'} = 6\ Rp * Cp + 2\ Rp * Cres.$

By comparison, the proposed MRP has the same parasitic RC with the selected path in TMUX, while RRT has more parasitic RC. The excessive parasitic RC in RRT may slow down the discharging of the reference path, making the sense amplifier prone to output resistancemargin between the configuration bit and the reference resistor is subtle due to memory variation.

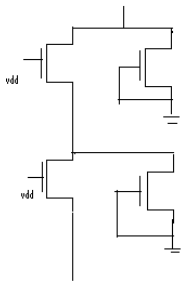

FIG 3. MATCHED REFERENCE PATH

3.3 FERRO ELECTIC RANDOM-ACCESS MEMORY (FRAM)

Different from crossbar array, a 1T1C FRAM cell can eliminate the sneaking current and the disturbances during write and read, thus saving power and acquiring high yield. The typical CON and COFF of FRAM are of kilo-ohms and megaohms, respectively , and ROFF/RON is over 100, which is at least 40× larger than that of MRAM . Therefore, sufficient sense margin is guaranteed and the configuration resources are also saved by half compared with the parallel

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or serial combination scheme . Moreover, the FRAM storage layer, i.e., C0-3 and Cref , is stacked in the back-end of line without occupying an additional area. Because the characteristics of FRAM are different from conventional resistor, the sense margins of CON and COFF compared with a conventional reference resistor may suffer asymmetric changes under memory and logic process variation, which may result in read failure. To resolve this issue, dummy FRAM cell, which is programmed to a mid-state resistance, is adopted as the reference resistor. Thus, the configuration bits and reference capacitor .vary in the same way across different temperatures and process conditions, preserving the sense margins for both Con and Coff. Moreover, the dummy cell occupies less area than conventional peripheral decoding and writing circuits for dummy cell can also be shared with configuration bits, bringing less area overhead. In our proposed nvLUT, since WL, BL, and SL are all drawn out from the FRAM slice, both unipolar and bipolar FRAM can be programmed by enforcing set or reset voltage on BL or SL while activating the corresponding WL. Because the dummy FRAM cell with a mid-state resistance is used as the reference, the adopted FRAMs should support the trimming of its storage capacitors to a specific value. In this brief, in order to evaluate our proposed nvLUT.

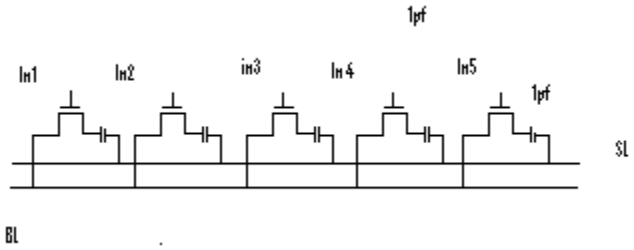
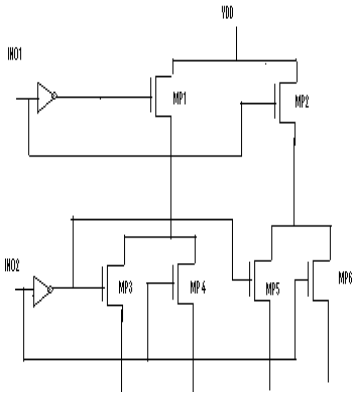


FIG 4: FRAM

3.4 TERMINAL MULTIPLEXER (TMUX)

A terminal multiplexer is a software application that can be used to multiplex several virtual consoles, allowing a user to access multiple separate login sessions inside a single terminal window, or detach and reattach sessions from a terminal. It is useful for dealing with multiple programs from a command line interface, and for separating programs from the session of the Unix shell that started the program, particularly so a remote process continues running even when the user is disconnected. tmux is a program which allows multiple text terminal (TTY) processes to be created and managed from a single text terminal. The set of processes running in tmux may be detached from the terminal, continue running in the background and reattached to a different terminal without interruption. It provides the ability to display output on disparate terminals simultaneously and a large set of feature.



FERROMAGNETIC MEMORY:

A fRAM is a device that can switch between one or more resistances under the application of appropriate voltages. Devices can have two or more discrete resistance states, or may have a continuously variable resistance. Whatever the case, it is important that the change in resistance is governed by the past history of the device - that is, by the previous voltage applied, or the previous current that has flowed through the device. Crossbar boasts that its FRAM storage solution is capable of storing up to 1TB of data on a single chip, thanks to the ability of "3D-stacking" multiple cells in different configurations in order to save space while still upping the storage limits. All of this can fit into a tight, tiny space, which could then fit into mobile devices. The company also says that the new chip technology consumes less energy (approximately 20 times less), extending battery life in devices "to weeks, months, or years." Speed wise, Crossbar claims that FRAM has a write speed that's 20 times faster than NAND memory (around 140MB/s, compared

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to 7MB/s with NAND), and is 10 times more reliable as well, noting that it "approaches DRAM reliability" levels. Read speeds are said to be around 17MB/s.

Advantages of ferro electric RAM

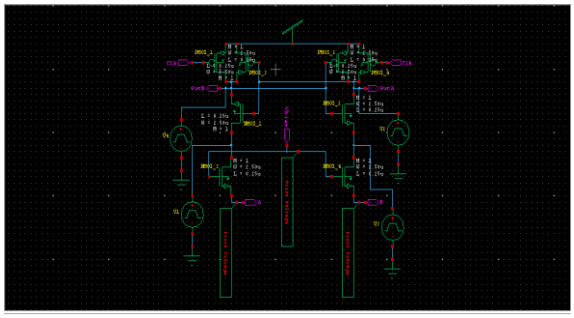
Highest Capacity: Up to 1TB of storage on a single chip; multiple terabytes with 3D stacking
Lowest Power: Extends Battery Life to Weeks, Months, or Years
Highest Performance: 20x faster write than NAND
Easiest SoC Integration: Simple stacking on logic in standard CMOS at most advanced nodes
Most Reliable: 10x the endurance of NAND, approaching DRAM reliability

FRAM Performance

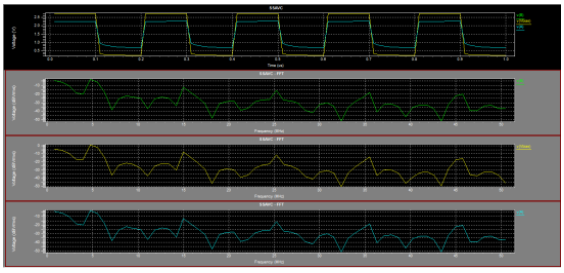
The first row indicates the switching type. As can be seen most of the devices show the bipolar switching feature. As discussed earlier, bipolar device generally has less RESET current than unipolar device and therefore is more power efficient. The next two entries are device structure and cell area which both are related to scaling properties of FRAM and will be discussed in next section. Here, several important device performance characteristics such as speed, endurance, retention and HRS/LRS ratio are introduced. Speed is the time needed to program and erase the memory device. In this case, it is the minimum time required to establish and annihilate the conductive filament inside FRAM. Nowadays the demonstrated speed of FRAM is less than 10ns which is much faster than that of Flash (in tens of µs range). In addition, the operating voltage for a typical Flash is at least larger than 5 volts, whereas only less than 2V is required for FRAM.

4. SIMULATION RESULTS

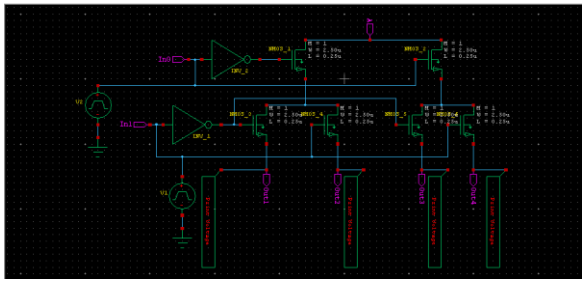
SSAVC (single stage amplifier voltage clamp transistor):



OUTPUT SSAVC



TMUX diagram:



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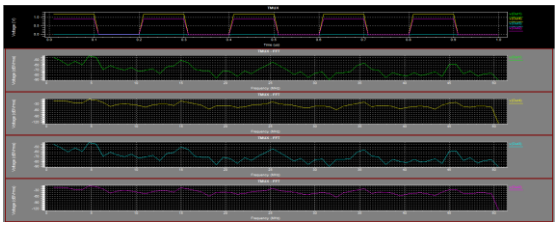
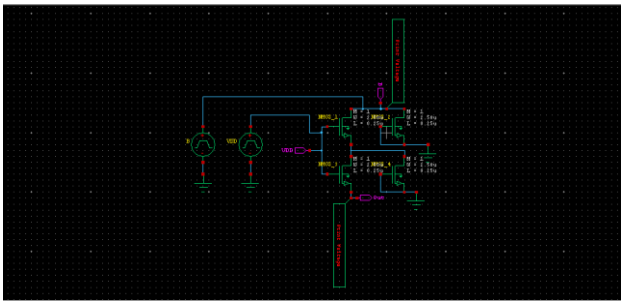
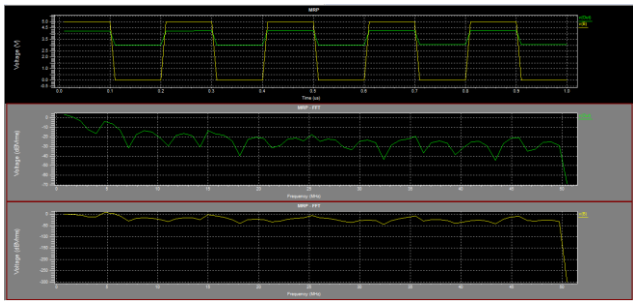
OUTPUT TMUX:



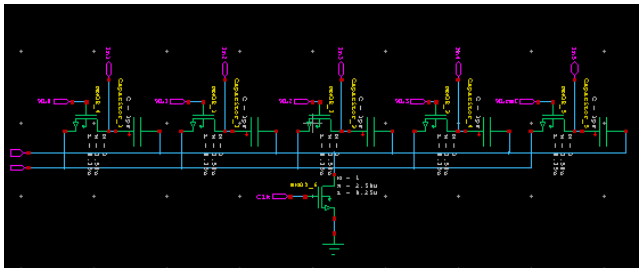
MRP DIAGRAM



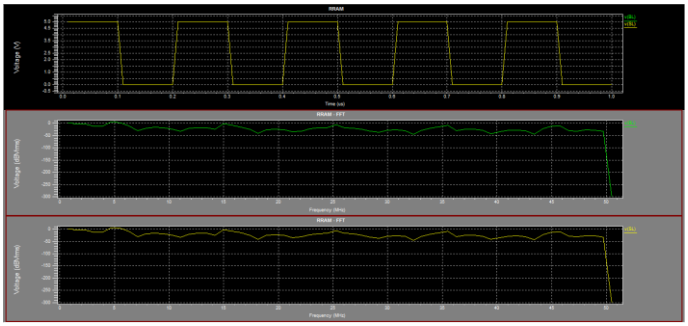
OUTPUT MRP



FRAM SLICE:



OUTPUT:



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POWER CONSUMPTION

NON VOLATILE MEMORY	VDD	VBIAS
FRAM	1.075956e-004 watts	1.250535e-006 watts
RRAM	1.38604e-004 watts	5.08994e-006watts

CONCLUSION

The design techniques of low-power variation-tolerant nvLUT are described in this brief. FRAM is adopted as the configuration bit and the reference resistor to provide large sense margin, thus alleviating the effects of memory and logic process variations. Because of the high COFF/CON of FRAM, SSAVC helps to reduce the power and area without impairing the reliability. The MRP is also devised to reduce the parasitic RC mismatch between the selected path in the multiplexer and the reference path for reliable operation. By evaluation, remarkable improvements in power, delay, area, and reliability are achieved.

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